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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,676	12/14/2001	Shahram Abdollahi-Alibeik	204.1001.02	9559

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EXAMINER	
BATAILLE, PIERRE MICHE	
ART UNIT	**PAPER NUMBER**
2186	4

DATE MAILED: 04/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/017,676	Applicant(s) ABDOLLAHI-ALIBEIK ET AL.	
	Examiner Pierre-Michel Bataille	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification/Claim Objection

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors.

2. The disclosure is objected to because of the following informalities:

Claim 1:

The recitation "received on one of said input interfaces" is unclear or it is not clear how it relates to "at least one input interface", supposed the "at least one" is simply one.

It appears that "a routing treatment said router is capable of applying to said message" would be amended for clarification. It appears that "a routing treatment to which said router is capable of applying said message" would better clarify the claimed language.

Claim 4, reciting "each prefix length of said input value" lack antecedent basis in the claim. It appears that the claims should recite dependency upon claim 3.

Claim 5, reciting, "at least one of said each prefix length" lack antecedent basis in the claim. It appears that the claims should recite dependency upon claim 3.

Please note that these are merely exemplary. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-9 are rejected under 35 U.S.C. 102(a) as being anticipated by "**A design for high-speed low-power CMOS fully parallel content-addressable memory macros**" (Miyatake et al).

With respect to claim 1, Miyatake teaches high-speed Low-Power content addressable memory providing fast look-up table for used in network switches and routers, comprising: at least one input interface and at least one output interface (input address and data ports and output address and data ports, Fig. 1; Col. 2, page 957), said router being coupled to a plurality of content addressable memory banks, each memory banks being independently responsive to an input value, said input value being responsive to a message (plurality of memory cell arrays subdivided into sub-arrays such that the input reference data being searched is sent to all memory locations activating all cell arrays for data comparison at the same time) [Col. 2; page 956; Col. 1, page 958].

With respect to claim 2, Miyatake teaches said routing apparatus including a plurality of monolithic integrated devices (plurality of ASIC chips) each including a plurality of content addressable memory banks, each memory bank being independently responsive to said input value (input reference data being searched is sent to all memory locations activating all cell arrays for data comparison at the same time) [Col. 2; page 956; Col. 1, page 958].

With respect to claims 3-6, Miyatake teaches each memory bank being associated with a selected prefetch length each associated with one integrated device [Col. 1, page 958].

With respect to claims 7-9, Miyatake teaches set of entries including continuous address range and a set of routing information [Col. 2, page 957].

5. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6,665,297 (Hariguchi et al).

With respect to claim 1, Hariguchi teaches a network routing system, comprising: at least one input interface and at least one output interface (input ports and output ports, Fig. 2A, 2B; Col. 2, page 957), a router being coupled to a plurality of content addressable memory banks, each memory banks being independently responsive to an input value, said input value being responsive to a message (the router comprising a content addressable memory storing a plurality of data pairs or lookup table in parallel such that all lookup tables are configured to perform address lookup operation simultaneously) [Fig. 2A, 2B; Col. 5, Lines 50-59].

With respect to claim 2, Hariguchi teaches said routing apparatus including a plurality of monolithic integrated devices (plurality of ASIC chips) each including a plurality of content addressable memory banks, each memory bank being independently responsive to said input value (the router comprising a content addressable memory storing a plurality of data pairs or lookup table in parallel such that all lookup tables are configured to perform address lookup operation simultaneously) [Col. 5, Lines 50-59].

With respect to claims 3-6, Hariguchi teaches each memory bank being associated with a selected prefetch length each associated with one integrated device (each lookup table being associated with a distinct prefix length) [Col. 5, Lines 52-55].

With respect to claims 7-9, Hariguchi teaches set of entries including continuous address range and a set of routing information [Col. 3, Lines 32-45].

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

McAuley, A. et al., Fast routing table lookup using CAMs, IEEE, pp. 1382-1391, 1993.

Miyatake, H et al. A design for high-speed low-power CMOS fully parallel content-addressable memory macros, IEEE Journal of Solid-State Circuits, Volume: 36, Issue: 6, pp. 956 – 968, June 2001.

US 5,938,736 (Muller et al) teaching search engine architecture for a high performance multi-layer switch element.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (703) 305-0134. The examiner can normally be reached on Tue-Fri (7:30A to 6:00P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Pierre-Michel Bataille
Primary Examiner
Art Unit 2186

April 23, 2004